

WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, comprising the steps of:
 - forming an amorphous layer in a region from a surface of a semiconductor region to a first depth;
 - 5 by heat treating the amorphous layer at a prescribed temperature, restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth; and
 - forming a pn junction at a third depth that is shallower than the second depth by introducing ions into the heat-treated amorphous layer.
- 10 2. The manufacturing method of a semiconductor device according to claim 1, wherein the prescribed temperature is in a range of 475°C to 600°C.
- 15 3. The manufacturing method of a semiconductor device according to claim 1, wherein the third depth is in a range of 5 nm to 15 nm.
4. The manufacturing method of a semiconductor device according to claim 1, wherein a pattern of a gate electrode that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region.
- 20 5. A method for manufacturing a semiconductor device, comprising the steps of:
 - forming an amorphous layer in a region from a surface of a semiconductor region of a first conductivity type to a first depth;
 - by heat treating the amorphous layer at a prescribed temperature, restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is

shallower than the first depth so that the amorphous layer shrinks to the second depth;
forming a first impurity layer of a second conductivity type which has a pn junction
at a third depth that is shallower than the second depth by introducing ions into the heat-
treated amorphous layer; and

5 activating the first impurity layer.

6. The manufacturing method of a semiconductor device according to claim 5,
wherein the third depth is in a range of 5 nm to 15 nm.

10 7. The manufacturing method of a semiconductor device according to claim 5,
wherein the prescribed temperature is in a range of 475°C to 600°C, and the activation of
the first impurity layer is conducted in a temperature range of 500°C to 700°C.

8. The manufacturing method of a semiconductor device according to claim 5,
15 wherein a pattern of a gate electrode that is formed on the semiconductor region is non-
uniformly distributed on the semiconductor region.

9. A method for manufacturing a semiconductor device, comprising the steps of:
forming a gate electrode on a semiconductor region of a first conductivity type;
20 forming an amorphous layer in a region from a surface of the semiconductor region
of the first conductivity type to a first depth;
by heat treating the amorphous layer at a prescribed temperature, restoring a crystal
structure of the amorphous layer in a region from the first depth to a second depth that is
shallower than the first depth so that the amorphous layer shrinks to the second depth;
25 forming a first impurity layer of a second conductivity type which has a pn junction

at a third depth that is shallower than the second depth by introducing ions into the heat-treated amorphous layer;

- forming a second impurity layer of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by
- 5 introducing ions into the heat-treated amorphous layer; and
- activating the first impurity layer and the second impurity layer.

10. The manufacturing method of a semiconductor device according to claim 9, wherein the third depth is in a range of 5 nm to 15 nm.

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11. The manufacturing method of a semiconductor device according to claim 9, wherein the prescribed temperature is in a range of 475°C to 600°C, and the activation of the first impurity layer and the second impurity layer is conducted in a temperature range of 500°C to 700°C.

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12. The manufacturing method of a semiconductor device according to claim 9, wherein a pattern of a gate electrode that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region.

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13. A method for manufacturing a semiconductor device, comprising the steps of:

forming a gate electrode on a semiconductor region of a first conductivity type;

forming an amorphous layer in a region from a surface of the semiconductor region to a first depth;

forming an insulating sidewall on a side surface of the gate electrode while

25 restoring a crystal structure of the amorphous layer in a region from the first depth to a

second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth, the restoration of the crystal structure of the amorphous layer being caused by heat treatment of a prescribed temperature which is conducted during formation of the sidewall;

- 5 forming a first impurity layer of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions on both sides of the gate electrode in the heat-treated amorphous layer; and
activating the first impurity layer.

10 14. The manufacturing method of a semiconductor device according to claim 13, further comprising the step of:

after the step of forming the first impurity layer, forming a second impurity layer of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions on both sides of the gate 15 electrode in the amorphous layer, wherein

the second impurity layer is simultaneously activated in the step of activating the first impurity layer.

15 15. The manufacturing method of a semiconductor device according to claim 13,
20 wherein the first impurity layer has a depth of 5 nm to 15 nm.

16. The manufacturing method of a semiconductor device according to claim 13, wherein the prescribed temperature is in a range of 475°C to 600°C, and the activation is conducted in a temperature range of 500°C to 700°C.

17. The manufacturing method of a semiconductor device according to claim 13, wherein a pattern of a gate electrode that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region.